**Sirius whole chip test**

Revision history

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| --- | --- | --- | --- |
| Revision | Date | Description | Author |
| 0.1 | 2017-03-28 | Initial | Songpan |
| 0.2 |  |  |  |
|  |  |  |  |

# Overview

## Introduce

Sirius project need support below test:

1. DFT test
2. MBIST test
3. Boundary scan test
4. ATE function test , including OTP CP test

# DFT/test

## Test mode configure and hookup pin list

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| PAD name | TEST\_MODE\_EN | PWM0 | PWM1 | PWM3 | GP0 | RSTN | comment |
| function name | TEST\_MODE\_EN | CFG\_PIN[0] | CFG\_PIN[1] | CFG\_PIN[2] | GPIO\_0 | RSTN |
| function mode | 0 | x | x | x | x | RSTN | function mode |
| scan mode | 1 | 1 | 0 | 0 | scan\_reset | RSTN | add scan reset from IO pad per DFT request |
| ate test mode | 1 | 0 | 1 | 0 | x | RSTN | IP analog PHY test mode |
| mbist mode | 1 | 0 | 0 | 1 | x | RSTN | mbist mode |
| bsd mode | 1 | 1 | 1 | 1 | x | RSTN | boundary scan mode |

## Test scheme for special block

### Support separate mbist test and result for the below blocks, which can be easily to screen chip if memory yield issue.

* Baseband block
* CEVA block
* HEVC
* ISP